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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,719	11/02/2001	Nigel C. Paver	INTL-0650-US (P12391)	3525

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,719	PAVER, NIGEL C.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,7, 12,13,15, 17, 19,22-24,26,28,31, 33 -45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7, 12,13,15, 17, 19,22-24,26,28,31, 33 -45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1,6,7, 12,13,15, 17, 19,22-24,26,28,31, 33 -45 remain for examination. Claims 2-5,8-11,14,16,18 , 20, 21,25, 27, 29,30, 32, have been canceled.

2. Applicant's arguments with respect to claims 1,6,7, 12,13,15, 17, 19,22-24,26,28,31, 33 -45 rejected under 35 U.S.C. 103(a) as being unpatentable over Buchholz (4,740,893) in view of Carnevale et al. (5,471,626) have been considered but are moot in view of the new ground(s) of rejection. However, response to applicant's remark on claim 13 under "101" will be addressed herein.

3. Claim 13 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reason given below.

4. As to claim 13, the rejection under 101 has been maintained and incorporated by reference the paragraph 6 in the last office action on 03/17/06. The response on 06/07/06 regarding the rejection on claim 13 under "101" has been fully considered but is not persuasive. Claim 13 additionally amended save the content of the registers to a memory. However, no substantial practical application can be found in the claim. The purpose of saving the contents of the register into memory is not clear. Therefore, it is not useful. The rejections under "101" to claim 1,19 have been withdrawn because refrain or not to transfer the content of the register on the update condition has a practical application.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,6, 7, 12,13,15,17,19,21,24,26,28,31,33,36,38,40,44,45 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan (5,488,709).

6. As to claim 1, 7, Chan taught a computer-implemented method comprising:

a) determining in a processor whether data in a first portion [data word] of a register [116] of the processor has been updated (see fig.15, register 116 valid bit set in col.33, lines 45-68; see also the valid bit set when the data line is written in col.8, lines 25-43);

b) if the data in the first portion [data word] of the register is updated, setting an indicator bit of an update (see valid bit);

c) indicator storage [valid] within a second portion of the register [116] to indicating the update;

d) if the data in the first portion [data word] has not yet updated refraining from transferring the contents of the register [116] back to a memory [RAM] based on the indicator bit (see condition of valid bit not met in col.33, lines 45-68).

7. As to claims 6, 44, Chan also included a single bit (see valid bit in col.8, lines 25-28).

8. As to claim 12 , see the valid set condition to update the data into RAM in col.33, lines 45-68).

9. As to claim 13, 17, Chan also taught :

a) a register (see fig.15, [116]); and

b) a storage storing instructions executed by the processor to determine whether the register has been updated and if the register is updated, set the indicator bit within an update status storage within the register and save the contents of register [116] to a memory [RAM (see col.33, lines 45-68).

10. As to claim 15, Chan also refrained from transferring the content to the memory [RAM] (see valid condition not set in col.33, lined 45-68).

As to claim 41, claim 41 is dependent form canceled clam, Correction is suggested in next response. see the connection between cpu and cache memory in the overall system in figs. 6,7 and fig.4.

11. As to claim 19,22, Chan also taught :

a) a processor having a register (see fig.15 register 116);

b) a storage to store instructions for execution by the system to determine whether the register has been updated and if the register has been updated set an indicator bit [valid] within an update status storage within the register [116] and to not transfer content of the register to a memory on a context change if the indicator bit is not set;

(see valid condition not met in col.33, lines 45-68).

c) an interface coupled between said memory and the processor (see the connection between cpu and cache memory in the overall system in figs. 6,7 and fig.4).

12. As to claim 23, see the content of register 116 updated back to RAM in col.33, lines 45-68.

13. As to claim 24,28, see context change in valid bit in col.33, lines 45-68.

14. As to claims 26 ,31, 33, see control register 116 in fig.15.

15. As to claims 36, 38,40, see the setting of valid indicator bit in fig.15 [116] and col.33, lines 55- 68.

16. As to claim 45, Chan also taught not to transfer of the contents of the register to memory if not updated, otherwise transferring the content to the memory (see the updated of the register content to RAM in col.33, lines 45-68, see also the valid not set condition for not to transfer the content of the register).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 34,37,39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan (5,488,709) in view of Russel (6,751,737) .

18. As to claims 34,37,39, limitations of parent clams have been discussed above, and it will not be repeated herein. Chan did not specifically showed the context switch as claimed . However, Russel taught a clearing of an indicator (MVM context register 128) upon occurrence of context switch (see the data in MVM context register 128 indicating whether the execution environment was initialized upon the election of first context in col.7, lines 39-52, see also the background of context switch in col.1, lines 10-15,50-61 , see also MVM context switching in col.2, lines 46-54).

19. It would have been obvious to one of ordinary skill in the ad o use Russel in Chan for including the clearing the of the indicator upon the context switch as claimed because the use of Russell could provide Chan the control capability to accept different system conditions at a predefined processing parameters (e.g. the context switching) , and therefore, increasing the flexibility of Chan, and because Chan did disclose the resuming the execution after until the write was completed (see col.3, lines 43-55), and therefore, provide a suggestion of the need of a context switch in order to recover the processing state of the system.

20. Claims 35,42,43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan ((5,488,709) in view of Dynarski et al. (6,628,671).

21. As to claims 35,42,43, Chan did not specifically show the power consumption of battery operation as claimed. However, Dynarski disclosed a system including a battery operated system (see the context switching in abstract, see also the laptop computer in

Col.1, lines 5- 37). It would have been obvious to one of ordinary skill in the art to use Dynarski in Chan for reducing the power consumption as claimed because the use of Dynarski could provide the control ability of Chan to enable the system based on the activities of system , and therefore, minimizing the power consumption on idle processing cycle, and because Chan also disclosed the resuming the execution after until the write was completed (see col.3, lines 43-55), which was a suggestion of the need for using the battery operated system for reducing the power consumption before the processor resumed the execution, and in doing so, provided a motivation.

22. Claims 1,7,19 are rejected under 35 U.S.C. 102(b) as being anticipated by Leedom et al. (6,012,135).

23. As to Claim 1,7, 19, Leedom taught a computer-implemented method comprising:

A) determining in a processor whether data in a first portion (see 802, 806, 808) of a register [810] of the processor has been updated (see the valid bit indication of the valid s condition for performing activity in col.14, lines 35-46);

b) if the data in the first portion (see 802, 806, 808) of the register is updated, setting an indicator bit [804 v bit] of an update indicator storage within a second portion [804] of the register to indicate the update (see the validity condition in col.14, lines 35-46);

c) if the data in the first portion [804 v] has not yet updated, refraining (or not transferring to a memory), from transferring the contents of the register back to a memory (see the single store after load in col.14, lines 62-67, col.15, lines 1-8, see also the stop of the second store instruction) based on the indicator bit (see the activity registers).

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a)Masuda et al. (6,933,651) is cited for the teaching of the updated bit indication in a register (see col.48, lines 35-46) .

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
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